B) 8PW

Sterne Kessler Goldstein Fox
ATTORNEYS AT LAW

April 12, 2005

WRITER'S DIRECT NUMBER:
(202) 772-8645
INTERNET ADDRESS:
JASONE@SKGF.COM

Commissioner for Patents
PO Box 1450
Alexandria, VA 22313-1450

Mail Stop Office of Initial Patent Examination's Filing Receipt Corrections
Art Unit 2817

Re: U.S. Utility Patent Application
Application No. 09/972,019; Filed: October 5, 2001
For: **Low Offset and Low Glitch Energy Charge Pump for PLL-Based Timing Recovery Systems**
Inventor: Myles H. Wakayama
Our Ref: 1875.2070002

Sir:

Transmitted herewith for appropriate action are the following documents:

1. Request for Corrected Official Filing Receipt attaching: (a) a copy of the priority data for 60/101555, (b) a copy of the priority data for 09/649197, (c) a copy of priority data for 09/398101, and (d) a Copy of Preliminary Amendment previously filed on March 22, 2002 showing a correct chain of priority on page 2;

2. Photocopy of the instant Official Filing Receipt with corrections; and

3. One (1) return postcard.

It is respectfully requested that the attached postcard be stamped with the date of filing of these documents, and that it be returned to our courier. In the event that extensions of time are necessary to prevent abandonment of this patent application, then such extensions of time are hereby petitioned.

The U.S. Patent and Trademark Office is hereby authorized to charge any fee deficiency, or credit any overpayment, to our Deposit Account No. 19-0036.

Respectfully submitted,

STERNE, KESSLER, GOLDSTEIN & FOX P.L.L.C.

Jason D. Eisenberg
Attorney for Applicant
Registration No. 43,447

JDE/lvt
385978_1.DOC

IN THE UNITED STATES PATENT AND TRADEMARK OFFICE

In re application of:	Confirmation No.: 3152
Myles H. Wakayama	Art Unit: 2817
Appl. No.: 09/972,019	Examiner: Arnold Kinkead
Filed: October 5, 2001	Atty. Docket: 1875.2070002
For: **Low Offset and Low Glitch Energy Charge Pump for PLL-Based Timing Recovery Systems**	

Request for Corrected Official Filing Receipt

Commissioner for Patents
PO Box 1450
Alexandria, VA 22313-1450

Attn: Office of Initial Patent
Examination's Filing
Receipt Corrections

Sir:

Applicant hereby requests that a corrected Official Filing Receipt be issued and sent to the undersigned representative. Specifically, the following corrections to the Official Filing Receipt are requested per the attached: (a) copy of the priority data for 60/101555, (b) copy of the priority data for 09/649197, (c) copy of priority data for 09/398101, and (d) Copy of Preliminary Amendment previously filed on March 22, 2002; copy of the Preliminary Amendment filed March 22, 2002: Under **"Domestic Priority data as claimed by applicant" please add after 6,326,852, "which is a continuation of 09/398,101 09/16/1999 PAT 6,181,210".** In support of the above request, a photocopy of the instant Official Filing Receipt is enclosed with the corrections noted in red. It is requested that a corrected Official Filing Receipt be issued, and sent to the undersigned at the earliest possible time.

Respectfully submitted,

STERNE, KESSLER, GOLDSTEIN & FOX P.L.L.C.

Jason D. Eisenberg
Attorney for Applicant
Registration No. 43,447

Date: April 12, 2005

1100 New York Avenue, N.W.
Washington, D.C. 20005-3934
(202) 371-2600
385969_1.DOC

UNITED STATES PATENT AND TRADEMARK OFFICE

COMMISSIONER FOR PATENTS
UNITED STATES PATENT AND TRADEMARK OFFICE
WASHINGTON, D.C. 20231
www.uspto.gov

APPLICATION NUMBER	FILING DATE	GRP ART UNIT	FIL FEE REC'D	ATTY.DOCKET.NO	DRAWINGS	TOT CLAIMS	IND CLAIMS
09/972,019	10/05/2001	2817	870	47426/RJP/B600	4	1	1

CONFIRMATION NO. 3152

UPDATED FILING RECEIPT

OC000000007338029

Sterne, Kessler, Goldstein & Fox P. L. L. C.
Suite 600
1100 New York Avenue, N. W.
Washington, DC 20005-3934

Date Mailed: 01/22/2002

Receipt is acknowledged of this nonprovisional Patent Application. It will be considered in its order and you will be notified as to the results of the examination. Be sure to provide the U.S. APPLICATION NUMBER, FILING DATE, NAME OF APPLICANT, and TITLE OF INVENTION when inquiring about this application. Fees transmitted by check or draft are subject to collection. Please verify the accuracy of the data presented on this receipt. **If an error is noted on this Filing Receipt, please write to the Office of Initial Patent Examination's Customer Service Center. Please provide a copy of this Filing Receipt with the changes noted thereon. If you received a "Notice to File Missing Parts" for this application, please submit any corrections to this Filing Receipt with your reply to the Notice. When the USPTO processes the reply to the Notice, the USPTO will generate another Filing Receipt incorporating the requested corrections (if appropriate).**

Applicant(s)

Myles H. Wakayama, Laguna Niguel, CA;

Domestic Priority data as claimed by applicant

THIS APPLICATION IS A CON OF 09/649,197 08/28/2000 PAT 6,326,852 Which is a CON of 09/398,101 09/16/1999 PAT 6,181,210
WHICH CLAIMS BENEFIT OF 60/101,555 09/21/1998

Foreign Applications

If Required, Foreign Filing License Granted 11/05/2001

Projected Publication Date: 05/02/2002

Non-Publication Request: No

Early Publication Request: No

JAN 25 2002

MH RCS 1/25 2:25 mb

Title

Low offset and low glitch energy charge pump for PLL-based timing recovery systems

Preliminary Class

331

LICENSE FOR FOREIGN FILING UNDER
Title 35, United States Code, Section 184
Title 37, Code of Federal Regulations, 5.11 & 5.15

GRANTED

The applicant has been granted a license under 35 U.S.C. 184, if the phrase "IF REQUIRED, FOREIGN FILING LICENSE GRANTED" followed by a date appears on this form. Such licenses are issued in all applications where the conditions for issuance of a license have been met, regardless of whether or not a license may be required as set forth in 37 CFR 5.15. The scope and limitations of this license are set forth in 37 CFR 5.15(a) unless an earlier license has been issued under 37 CFR 5.15(b). The license is subject to revocation upon written notification. The date indicated is the effective date of the license, unless an earlier license of similar scope has been granted under 37 CFR 5.13 or 5.14.

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NOT GRANTED

No license under 35 U.S.C. 184 has been granted at this time, if the phrase "IF REQUIRED, FOREIGN FILING LICENSE GRANTED" DOES NOT appear on this form. Applicant may still petition for a license under 37 CFR 5.12, if a license is desired before the expiration of 6 months from the filing date of the application. If 6 months has lapsed from the filing date of this application and the licensee has not received any indication of a secrecy order under 35 U.S.C. 181, the licensee may foreign file the application pursuant to 37 CFR 5.15(b).

United States Patent and Trademark Office

PATENT APPLICATION INFORMATION RETRIEVAL

Search results for application number:09/649,197			
Application Number:	09/649,197	Customer Number:	-
Filing or 371(c) Date:	08-28-2000	Status:	Patented Case
Application Type:	Utility	Status Date:	11-16-2001
Examiner Name:	GRIMM, SIEGFRIED H	Location:	FILE REPOSITO (FRANCONIA)
Group Art Unit:	2817	Location Date:	11-30-2001
Confirmation Number:	8486	Earliest Publication No:	-
Attorney Docket Number:	40244/RJP/B600	Earliest Publication Date:	-
Class/ Sub-Class:	331/017	Patent Number:	6,326,852
First Named Inventor:	Myles Wakayama, Laguna Niguel, CA	Issue Date of Patent:	12-04-2001
Title Of Invention:	Low offset and low glitch energy charge pump for pll-based ti recovery systems		

Select Search Option

File History
Maintenance Fees - Retrieve fees to pay
Maintenance Fees - View payment windows
Maintenance Statement - View 04 year payment window
Maintenance Statement - View 08 year payment window
Maintenance Statement - View 12 year payment window

Search

Maintenance Fees Available: Mon-Fri 5:30 AM to Midnight, Sat-Sun-Hol. 7:30 AM to 8:00 PM E.T.

Parent Continuity Data			
Description	Parent Number	Parent Filing or 371(c) Date	Parent Stat
This application is a Continuation of	09/398,101	09-16-1999	Patented
Which claims benefit of Provisional Application	60/101,555	09-21-1998	Expired

Child Continuity Data
09/972,019 filed on 10-05-2001 which is Pending claims the benefit of 09/649,1

United States Patent and Trademark Office

PATENT APPLICATION INFORMATION RETRIEVAL

Search results for application number: 60/101,555

Application Number:	60/101,555	Customer Number:	-
Filing or 371(c) Date:	09-21-1998	Status:	Provisional Application Ex
Application Type:	Provisional	Status Date:	09-21-2001
Examiner Name:	-	Location:	FILE REPOSIT((FRANCONIA)
Group Art Unit:	-	Location Date:	08-06-2001
Confirmation Number:	5000	Earliest Publication No:	-
Attorney Docket Number:	148470-0047	Earliest Publication Date:	-
Class/ Sub-Class:	-/-	Patent Number:	-
First Named Inventor:	MYLES WAKAYAMA, LAGUNA NIGUEL, CA (US)	Issue Date of Patent:	-
Title Of Invention:	LOW OFFSET AND LOW GLITCH ENERGY CHARGE PUMP DE:		

Select Search Option

File History Search

Parent Continuity Data

Description	Parent Number	Parent Filing or 371(c) Date	Par(
No Parent Continuity Data Found.			

Child Continuity Data

09/398,101 filed on 09-16-1999 which is Patented claims the benefit of 60/101,5
09/649,197 filed on 08-28-2000 which is Patented claims the benefit of 60/101,5
09/972,019 filed on 10-05-2001 which is Pending claims the benefit of 60/101,5

United States Patent and Trademark Office

PATENT APPLICATION INFORMATION RETRIEVAL

Search results for application number:09/398,101			
Application Number:	09/398,101	Customer Number:	-
Filing or 371(c) Date:	09-16-1999	Status:	Patented Case
Application Type:	Utility	Status Date:	01-11-2001
Examiner Name:	GRIMM, SIEGFRIED H	Location:	FILE REPOSIT (FRANCONIA)
Group Art Unit:	2817	Location Date:	01-29-2001
Confirmation Number:	9630	Earliest Publication No:	-
Attorney Docket Number:	35870/JWE/B6	Earliest Publication Date:	-
Class/ Sub-Class:	331/008	Patent Number:	6,181,210
First Named Inventor:	MYLES H. WAKAYAMA, LAGUNA NIGUEL, CA (US)	Issue Date of Patent:	01-30-2001
Title Of Invention:	LOW OFFSET AND LOW GLITCH ENERGY CHARGE PUMP FOI BASED TIMING RECOVERY SYSTEMS		

Select Search Option

File History
Maintenance Fees - Retrieve fees to pay
Maintenance Fees - View payment windows
Maintenance Statement - View 04 year payment window
Maintenance Statement - View 08 year payment window
Maintenance Statement - View 12 year payment window

Search

Maintenance Fees Available: Mon-Fri 5:30 AM to Midnight, Sat-Sun-Hol. 7:30 AM to 8:00 PM E.T.

Parent Continuity Data			
Description	Parent Number	Parent Filing or 371(c) Date	Parent Stat
This application claims benefit of Provisional Application	60/101,555	09-21-1998	Expired

Child Continuity Data
09/649,197 filed on 08-28-2000 which is Patented claims the benefit of 09/398,'

IN THE UNITED STATES PATENT AND TRADEMARK OFFICE

In re application of:	Confirmation No.: 3152
Myles H. Wakayama	Art Unit: N/A
Appl. No. 09/972,019	Examiner: N/A
Filed: October 5, 2001	Atty. Docket: 1875.2070002
For: **Low Offset and Low Glitch Energy Charge Pump for PLL-Based Timing Recovery Systems**	

Preliminary Amendment

Box Non-Fee Amendments
Commissioner for Patents
Washington, D.C. 20231

Sir:

Applicant submits the following Amendment and Remarks. This Amendment is provided in the following format:

(A) A clean version of each replacement paragraph/section/claim along with clear instructions for entry;
(B) Starting on a separate page, appropriate remarks and arguments. 37 C.F.R. § 1.111 and MPEP 714; and
(C) Starting on a separate page, a marked-up version entitled: "Version with markings to show changes made."

It is not believed that extensions of time or fees for net addition of claims are required beyond those that may otherwise be provided for in documents accompanying this paper. However, if additional extensions of time are necessary to prevent abandonment of this application, then such extensions of time are hereby petitioned under 37 C.F.R. § 1.136(a), and any fees required therefor (including fees for net addition of claims) are hereby authorized to be charged to our Deposit Account No. 19-0036.

Amendments

In the Specification:

Please substitute the following paragraphs/sections for the pending paragraphs/sections.

Please replace the paragraph on Page 1, lines 7 - 10, with the following new paragraph:

--This application is a continuation of application Serial No. 09/649,197, filed August 28, 2000, now Patent 6,326,852, entitled LOW OFFSET AND LOW GLITCH ENERGY CHARGE PUMP FOR PLL-BASED TIMING RECOVERY SYSTEMS, which is a continuation of 09/398,101, filed September 16, 1999, now Patent 6,181,210, entitled LOW OFFSET AND LOW GLITCH ENERGY CHARGE PUMP FOR PLL-BASED TIMING RECOVERY SYSTEMS, and which is related to provisional application Serial No. 60/101,555, filed September 21, 1998, entitled LOW OFFSET AND LOW GLITCH ENERGY CHARGE PUMP DESIGN, all commonly owned by the Assignee of the present invention.--

Replace the paragraph beginning on Page 2, line 27, and ending on Page 3, line 8, with the following new paragraph:

--The data signal is received at a data input of the phase detector 10, in which the occurrence of the data's rising edge (its phase) is compared in time to the occurrence of a rising edge (the phase) of an output signal of the VCO 14. Conventionally, the phase detector incorporates logic circuitry (in effect a logical XNOR function) which precludes an output signal from being issued during phase comparisons unless two rising edges are present during a comparison cycle. This feature prevents the phase-lock-loop from becoming unstable by trying to perform a phase comparison between a VCO rising edge and a DATA ZERO bit (necessarily without a rising edge). It will be understood that the phase comparison result in such a situation would indicate either an infinite phase lead or an infinite phase lag, thus causing the VCO frequency to run out of control.--

On Page 3, replace the paragraph beginning on line 9 and ending on line 28 with the following new paragraph:

--According to convention, the phase detector 10 issues a PUMP UP signal 16 to the charge pump 12 if the datastream phase leads the VCO signal, and issues a PUMP DN 18 if the datastream phase lags the VCO signal. PUMP UP and PUMP DN are directed to the charge pump 12 which sources or sinks a particular amount of current (the pump current) to or from, respectively, the loop filter 13. Voltage is developed as the pump current is sourced or sunk, with the voltage being used to control the operational frequency of the VCO 14. The sign of the VCO control voltage variation depends on whether the phase of the datastream leads or lags the phase of the VCO output and its magnitude is a function of the extent of the phase lead or phase lag. Thus, the operational frequency of the VCO 14 is increased or decreased, as appropriate, to reduce the phase lead or phase lag of the inputs to the phase detector 10. The phase-lock-loop thus ensures that the VCO output, which is used as a timing reference, is locked in phase with the incoming serial datastream. Once the PLL is "locked", the timing reference signal (i.e., the VCO output) is used to control operation of a decision circuit 19 which defines regenerated or retimed data.--

On Page 9, replace the paragraph beginning on line 3 and ending on line 12 with the following new paragraph:

--In practical terms, lack of perfect symmetry between sourced and sunk charge pump current selectively adds a small component (a DC offset component, a glitch error component, or both) to the control voltage Vc provided to a VCO. These error components selectively shift frequency of a VCO relative to its nominal center frequency. Any offset from the center frequency will cause a phase detector's data capture window to shift, thus allowing a portion of data pulse position distribution to fall outside the detection window, and consequently increasing the system's bit error rate.--

Please replace the paragraph beginning on Page 11, line 28, through Page 12, line 4, with the following new paragraph:

--Similarly, the second current path, the right current path, is constructed of an upper P-channel transistor 50 and a lower N-channel transistor 52. The P-channel transistors 46 and 50 are mirror images of one another and have their source terminals connected together in common and to the pump-up current source 42. The lower N-channel transistors 48 and 52 are likewise mirror images of one another and also have their source terminals connected in common to the pump-down current source 44.--

On Page 12, replace the paragraph beginning on line 23 and ending on line 30 with the following new paragraph:

--An output node is defined by the common drain nodes of the P-channel and N-channel transistors defining one of the parallel current paths. Source and sink currents are output to an analog loop filter 54 constructed to include an RC network characterized by a resistor element 56 and a capacitor 58 which define the filter's zero. The RC network is coupled between the charge pump output and ground in parallel with a second capacitor 60 which defines the analog loop filter's pole.--

Replace the paragraphs beginning on Page 13, line 32 and ending on Page 14, line 20 with the following new paragraphs:

--Further, the transconductance amplifier 62 forces the common drain nodes of each of the current path of the charge pump 40 to be maintained at an equi-potential value with respect to one another. Thus, transconductance amplifier in combination with the "adjust" current source 63 functions to force the "down" current sunk by the "down" current source 44 to exactly equal the "up" current sourced by the "up" current source 42, in a manner independent of the output voltage of the charge pump. Thus, any DC mismatches between the "up" and "down" current sources which could cause offsets in the charge pump output, are removed. Since the charge pump output nodes are maintained at an equi-potential level, there is no further voltage dependence of the "up" and "down" current sources on the output voltage and DC offsets in the charge pump output are minimized.

It should be realized by one having skill in the art that the third "adjust" current source 63 need not be provided either as a separate element or in parallel with the "down" current source 44. In alternative embodiments, the "adjust" current source may receive a signal from the amplifier 62 and may be partially or wholly provided in parallel with the "pump-up" current source 42. In still other configurations the "adjust" current source 63 might be eliminated as a separate element and the amplifier 62 may be configured to control either the "pump-up" 42 or "pump-down" 44 current sources directly..--

On Page 15, replace the paragraph- beginning on line 16 and ending on line 22 with the following new paragraph:

--It will thus be recognized by those skilled in the art that various modifications may be made to the illustrated and other embodiments of the invention described above, without departing from the broad inventive scope thereof. It will be understood, therefore, that the invention is not -limited to the particular embodiments or arrangements disclosed, but is rather intended to cover any changes, adaptations or modifications which are within the scope and spirit of the invention as defined by the appended claims.--

In the Claims:

Please cancel claim 1 without prejudice or disclaimer.

Please add the following claims 24-44:

24. (New) A phase lock loop comprising:

a detector adapted to receive an input data signal;

a timing reference signal generator coupled to said detector; and

a charge pump coupled to said detector, said charge pump comprising:

first and second current sources;

first and second parallel current paths coupled at first ends to said first current source and coupled at second ends to said second current source, said first and second current paths having respective first and second output nodes;

a filter coupled to said first output node;

a capacitor coupled to said second output node; and

a feedback means coupled at a first input to said filter, at a second input to said capacitor, and at an output to one of said first and second current sources, said feedback means adapted to balance currents in said first and second current sources to minimize DC offset and glitch energy at a charge pump output node.

25. (New) The phase lock loop of claim 24, wherein said charge pump is implemented using CMOS technology.

26. (New) The phase lock loop of claim 24, wherein said feedback means is coupled to one of said first and second current sources via an adjusting current source.

27. (New) The phase lock loop of claim 24, wherein said feedback means is coupled directly to said first current source.

28. (New) The phase lock loop of claim 24, wherein said feedback means is coupled directly to said second current source.

29. (New) The phase lock loop of claim 24, wherein an adjusting current source is coupled between said feedback means and said first current source.

30. (New) The phase lock loop of claim 24, wherein an adjusting current source is coupled between said feedback means and said second current source.

31. (New) The phase lock loop of claim 24, wherein said filter is an analog loop filter.

32. (New) The phase lock loop of claim 24, wherein said feedback means is a transconductance amplifier.

33. (New) The phase lock loop of claim 24, wherein said filter comprises:

a resistor;

a first capacitor coupled in series with said resistor; and

a second capacitor coupled in parallel with said series resistor and first capacitor;

wherein an input to said feedback means is coupled to a node between said resistor and said first capacitor.

34. (New) The phase lock loop of claim 24, wherein said capacitor is a dump capacitor.

35. (New) The phase lock loop of claim 24, wherein said first current path comprises:

a first switching device; and

a second switching device;

wherein said first output node is located between said first and second switching devices.

36. (New) The phase lock loop of claim 35, wherein said first and second switching devices are transistors.

37. (New) The phase lock loop of claim 24, wherein said second current path comprises:

a first switching device; and

a second switching device;

wherein said second output node is located between said first and second switching devices.

38. (New) The phase lock loop of claim 37, wherein said first and second switching devices are transistors.

39. (New) A method of controlling a charge pump, the method comprising the steps of:

detecting an input signal and a timing reference signal with a detector, said detector then outputting a pump-up and pump-down signal;

receiving said pump-up and said pump-down signal at a charge pump;

transmitting said pump-up and said pump-down signals through first and second parallel current paths that are coupled between first and second current sources in said charge pump;

outputting a first current path output signal from said first current path to a filter, said filter producing a filter output signal;

outputting a second current path output signal from said second current path to a capacitor;

receiving said filter output signal and said second current path output signal at inputs of a feedback means, said feedback means generating a feedback output signal; and

balancing currents in said first and second current sources using said feedback output signal to minimize D.C. offsets and glitch energy.

40. (New) The method of claim 39, further comprising the step of directly adjusting said first current source with said feedback output signal.

41. (New) The method of claim 39, further comprising the step of directly adjusting said second current source with said feedback output signal.

42. (New) The method of claïm 39, further comprising the steps of:

receiving said feedback output signal at an adjusting current source; and

performing said balancing of said current in said first and second current sources via said feedback means and said adjusting current source.

43. (New) The method of claim 42, further comprising the step of coupling said adjusting current source directly to said first current source.

44. (New) The method of claim 42, further comprising the step of coupling said adjusting current source directly to said second current source.

45. (New) A method of controlling a charge pump having two parallel current paths formed of transistors, each current path coupled between a first current source and a second current source, said charge pump operating within a phase lock loop, the method comprising the steps of:

detecting a phase or frequency characteristic of an input signal to produce an output signal;

receiving said output signal at said charge pump and using said output signal to produce a charge pump control signal;

generating a characteristic current using one of said first current path and said second current path in response to said charge pump control signal; and

controlling a value of one of said first current source and said second current source to minimize D.C. offsets resulting from parasitic capacitances of said transistors.

In the Abstract:

Please replace the Abstract of the Disclosure with the new Abstract enclosed herewith on a separate page.

Remarks

Upon entry of the foregoing amendment, claims 24-45 are pending in the application, with 24, 39, and 45 being the independent claims. Claim 1 is sought to be cancelled without prejudice to or disclaimer of the subject matter therein. New claims 24-45 are sought to be added. These changes are believed to introduce no new matter, and their entry is respectfully requested.

The specification was amended in conformance with amendments made in the two previous above-mentioned applications and to add continuation data and more clearly discuss the invention. These changes are believed to introduce no new matter, and their entry is respectfully requested.

Applicant believes the present application is in condition for allowance. If the Examiner believes, for any reason, that personal communication will expedite prosecution of this application, the Examiner is invited to telephone the undersigned at the number provided. Prompt and favorable consideration of this Amendment is respectfully requested.

Respectfully submitted,

STERNE, KESSLER, GOLDSTEIN & FOX P.L.L.C.

Robert Sokohl
Attorney for Applicant
Registration No. 36,013

Date: 3/22/02

1100 New York Avenue, N.W.,
Suite 600
Washington, D.C. 20005-3934
(202) 371-2600

Version with markings to show changes made

The paragraph on Page 1, lines 7-10, is replaced with the following new paragraph:

--This application is a continuation of application Serial No. 09/649,197, filed August 28, 2000, now Patent 6,326,852, entitled LOW OFFSET AND LOW GLITCH ENERGY CHARGE PUMP FOR PLL-BASED TIMING RECOVERY SYSTEMS, which is a continuation of 09/398,101, filed September 16, 1999, now Patent 6,181,210, entitled LOW OFFSET AND LOW GLITCH ENERGY CHARGE PUMP FOR PLL-BASED TIMING RECOVERY SYSTEMS, and which is related to provisional application Serial No. 60/101,555, filed September 21, 1998, entitled LOW OFFSET AND LOW GLITCH ENERGY CHARGE PUMP DESIGN, which are all commonly owned by the Assignee of the present invention.--

The paragraph beginning on Page 2, line 27, and ending on Page 3, line 8, is replaced with the following new paragraph:

--The data signal is received at a data input of the phase detector 10, in which the occurrence of the data's rising edge (its phase) is compared in time to the occurrence of a rising edge (the phase) of an output signal of the VCO 14. Conventionally, the phase detector incorporates logic circuitry [circuity](in effect a logical XNOR function) which precludes an output signal from being issued during phase comparisons unless two rising edges are present during a comparison cycle. This feature [features] prevents the phase-lock-loop from becoming unstable by trying to perform a phase comparison between a VCO rising edge and a DATA ZERO bit (necessarily without a rising edge). It will be understood that the phase comparison result in such a situation would indicate either an infinite phase lead or an infinite phase lag, thus causing the VCO frequency to run out of control.--

The paragraph being on Page 3, line 9 and ending on line 28 is replaced with the following new paragraph:

--According to convention, the phase detector 10 issues a PUMP UP signal 16 to the charge pump 12 if the datastream phase leads the VCO signal, and issues a PUMP DN 18 if the datastream phase lags the VCO signal. PUMP UP and PUMP DN are directed to the charge pump 12 which sources or sinks a particular amount of current (the pump current) to or from, respectively, the loop filter 13. Voltage is developed as the -pump current is sourced or sunk, with the voltage being used to control the operational frequency of the VCO 14. The sign of the VCO control voltage variation depends on whether the phase of the datastream leads or lags the phase of the VCO output and its magnitude is a function of the extent of the phase lead or phase lag. Thus, the operational frequency of the VCO 14 is increased or decreased, as appropriate, to reduce the phase lead or phase lag of the inputs to the phase detector 10. The phase-lock-loop thus ensures that the VCO output, which is used as a timing reference, is locked in phase with the incoming serial datastream. Once the PLL is "locked", the timing reference signal (i.e., the VCO output) is used to control operation of a decision circuit 19 [16] which defines regenerated or retimed data.--

The paragraph beginning on Page 9, line 3 and ending on line 12 is replaced with the following new paragraph:

--In practical terms, lack of perfect symmetry between sourced and sunk charge pump current selectively adds a small component (a DC offset component, a glitch error component, or both) to the control voltage Vc provided to a VCO. These error components selectively shift frequency of a VCO relative to its nominal center frequency. Any offset from the center frequency will cause a phase detector's data capture window to shift, thus allowing a portion of data pulse position distribution to fall outside [out side] the detection window, and consequently increasing the system's bit error rate.--

The paragraph beginning on Page 11, line 28, through Page 12, line 4, is replaced with the following new paragraph:

--Similarly, the second current path, the right current path, is constructed of an upper P-channel transistor 50 and a lower N-channel transistor 52. The P-channel transistors 46 and 50 are mirror images of one another and have their source [drain] terminals connected together in common and to the pump-up current source 42. The lower N-channel transistors 48 and 52 are likewise mirror images of one another and also have their source terminals connected in common to the pump-down current source 44.--

The paragraph beginning on Page 12, line 23 and ending on line 30 is replaced with the following new paragraph:

--An output node is defined by the common drain nodes of the P-channel and N-channel transistors defining one of the parallel current paths. Source and sink currents are output to an analog loop filter 54 constructed to include an RC network characterized by a resistor element 56 and a capacitor 58 which define the filter's [filters] zero. The RC network is coupled between the charge pump output and ground in parallel with a second capacitor 60 which defines the analog loop filter's pole.--

The paragraphs beginning on Page 13, line 32 and ending on Page 14, line 20 are replaced with the following new paragraphs:

--Further, the transconductance amplifier 62 forces the common drain nodes of each of the current paths of the charge pump 40 to be maintained at an equi-potential value with respect to one another. Thus, transconductance amplifier in combination with the "adjust" current source 63 functions to force the "down" current sunk by the "down" current source 44 to exactly equal the "up" current sourced by the "up" current source 42, in a manner independent of the output voltage of the charge pump. Thus, any DC mismatches between the "up" and "down" current sources which could cause offsets in the charge pump output, are removed. Since the charge pump output nodes are maintained at an equi-potential level, there is no further voltage dependence of the "up" and "down" current sources on the output voltage and (further minimized) DC offsets in the charge pump output are minimized.

It should be realized by one having skill in the art that the third [thrid] "adjust" current source 63 need not be provided [n]either as a separate element[, n]or in parallel with the "down" current source 44. In alternative embodiments, [T]the "adjust" current source may receive a signal from the amplifier 62 and may [might also] be partially or wholly provided in parallel with the "pump-up" current source 42. In still other configurations [Further,] the "adjust" current source 63 might be eliminated as a separate element and the amplifier 62 may be configured to control either the "pump-up" 42 or "pump-down" 44 current sources directly.--

The paragraph beginning on Page 15, line 16 and ending on line 22 is replaced with the following new paragraph:

--It will thus be recognized by those skilled in the art that various modifications may be made to the illustrated and other embodiments of the invention described above, <u>without</u> [with out] departing from the broad inventive scope thereof. It will be understood, therefore, that the invention is not limited to the particular embodiments or arrangements disclosed, but is rather intended to cover any changes, adaptations or modifications which are within the scope and spirit of the invention as defined by the appended claims.

AMENDMENTS TO THE ABSTRACT OF THE DISCLOSURE
(Underlinings indicate insertions; brackets indicate deletions)

--**ABSTRACT** [OF THE DISCLOSURE]

LOW OFFSET AND LOW GLITCH ENERGY CHARGE PUMP
FOR PLL-BASED TIMING RECOVERY SYSTEMS

A high precision charge pump used in a phase-lock-loop incorporating a phase/frequency detector is designed and constructed to substantially eliminate the effects of DC offset and glitch errors on the charge pump output current. The high precision charge pump is constructed of parallel current paths each having a central node which is, in turn, connected to a feedback element. The feedback element defines a feedback current which is applied to the charge pump so as to maintain the two central [common drain] nodes at an equi-potential level and to maintain the value of the pump-down current exactly equal to the value of the pump-up current output by the device.--

The Abstract of the Disclosure is replaced by the following new Abstract:

LOW OFFSET AND LOW GLITCH ENERGY CHARGE PUMP
FOR PLL-BASED TIMING RECOVERY SYSTEMS

ABSTRACT

A high precision charge pump used in a phase-lock-loop incorporating a phase/frequency detector is designed and constructed to substantially eliminate the effects of DC offset and glitch errors on the charge pump output current. The high precision charge pump is constructed of parallel current paths each having a central node which is, in turn, connected to a feedback element. The feedback element defines a feedback current which is applied to the charge pump so as to maintain the two central nodes at an equi-potential level and to maintain the value of the pump-down current exactly equal to the value of the pump-up current output by the device.